

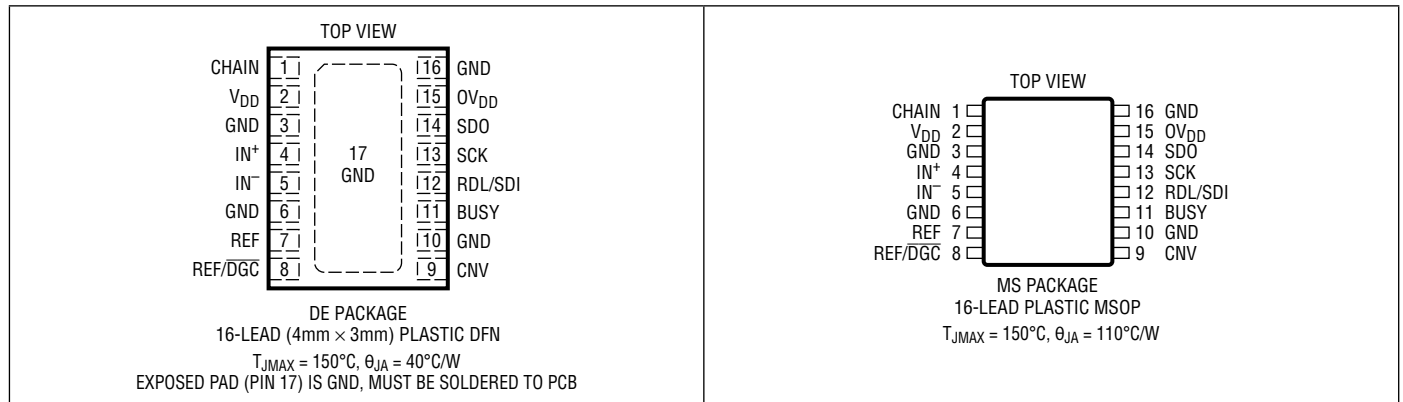
LTC2376-20

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD})	2.8V	Digital Output Voltage	
Supply Voltage (OV_{DD})	6V	(Note 3)	($GND - 0.3V$) to ($OV_{DD} + 0.3V$)
Reference Input (REF)	6V	Power Dissipation	500mW
Analog Input Voltage (Note 3)		Operating Temperature Range	
IN^+ , IN^-	($GND - 0.3V$) to ($REF + 0.3V$)	LTC2376C	0°C to 70°C
REF/ \overline{DGC} Input (Note 3)	($GND - 0.3V$) to ($REF + 0.3V$)	LTC2376I	-40°C to 85°C
Digital Input Voltage		Storage Temperature Range	-65°C to 150°C
(Note 3)	($GND - 0.3V$) to ($OV_{DD} + 0.3V$)		

PIN CONFIGURATION



ORDER INFORMATION <http://www.linear.com/product/LTC2376-20#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2376CMS-20#PBF	LTC2376CMS-20#TRPBF	237620	16-Lead Plastic MSOP	0°C to 70°C
LTC2376IMS-20#PBF	LTC2376IMS-20#TRPBF	237620	16-Lead Plastic MSOP	-40°C to 85°C
LTC2376CDE-20#PBF	LTC2376CDE-20#TRPBF	23760	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2376IDE-20#PBF	LTC2376IDE-20#TRPBF	23760	16-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>
For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN+}	Absolute Input Range (IN^+)	(Note 5) ●	-0.1		$V_{REF} + 0.1$	V
V_{IN-}	Absolute Input Range (IN^-)	(Note 5) ●	-0.1		$V_{REF} + 0.1$	V
$V_{IN+} - V_{IN-}$	Input Differential Voltage Range	$V_{IN} = V_{IN+} - V_{IN-}$ ●	$-V_{REF}$		$+V_{REF}$	V
V_{CM}	Common-Mode Input Range	●	$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
I_{IN}	Analog Input Leakage Current			0.01		μA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode		45 5		pF pF
CMRR	Input Common Mode Rejection Ratio	$f_{IN} = 125\text{kHz}$		86		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Resolution	●	20			Bits
	No Missing Codes	●	20			Bits
	Transition Noise			2.3		ppm_{RMS}
INL	Integral Linearity Error	(Note 6) $REF/DGC = GND$, (Note 6) ●	-2 -2	± 0.5 ± 0.5	2 2	ppm ppm
DNL	Differential Linearity Error	(Note 10) ●	-0.5	± 0.2	0.5	ppm
BZE	Bipolar Zero-Scale Error	(Note 7) ●	-13	0	13	ppm
	Bipolar Zero-Scale Error Drift			± 7		$\text{ppb}/^\circ\text{C}$
FSE	Bipolar Full-Scale Error	(Note 7) ●	-100	± 10	100	ppm
	Bipolar Full-Scale Error Drift			± 0.05		$\text{ppm}/^\circ\text{C}$

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ and $A_{IN} = -1\text{dBFS}$. (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$ ●	101	104		dB
SNR	Signal-to-Noise Ratio	$f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$ ● $f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$, $REF/DGC = GND$ ● $f_{IN} = 2\text{kHz}$, $V_{REF} = 2.5\text{V}$ ●	101 99 95.5	104 102 98		dB dB dB
THD	Total Harmonic Distortion	$f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$ ● $f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$, $REF/DGC = GND$ ● $f_{IN} = 2\text{kHz}$, $V_{REF} = 2.5\text{V}$ ●		-125 -125 -123	-115 -114 -113	dB dB dB
SFDR	Spurious Free Dynamic Range	$f_{IN} = 2\text{kHz}$, $V_{REF} = 5\text{V}$ ●	115	128		dB
	-3dB Input Bandwidth			34		MHz
	Aperture Delay			500		ps
	Aperture Jitter			4		ps
	Transient Response	Full-Scale Step		1		μs

REFERENCE INPUT The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{REF}	Reference Voltage	(Note 5)	● 2.5		5.1	V
I _{REF}	Reference Input Current	(Note 9)	●	0.24	0.3	mA
V _{IHDGC}	High Level Input Voltage REF/DGC Pin		● 0.8V _{REF}			V
V _{ILDGC}	Low Level Input Voltage REF/DGC Pin		●		0.2V _{REF}	V

DIGITAL INPUTS AND DIGITAL OUTPUTS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IH}	High Level Input Voltage		● 0.8 • OV _{DD}			V
V _{IL}	Low Level Input Voltage		●		0.2 • OV _{DD}	V
I _{IN}	Digital Input Current	V _{IN} = 0V to OV _{DD}	● -10		10	μA
C _{IN}	Digital Input Capacitance			5		pF
V _{OH}	High Level Output Voltage	I _O = -500μA	● OV _{DD} - 0.2			V
V _{OL}	Low Level Output Voltage	I _O = 500μA	●		0.2	V
I _{OZ}	Hi-Z Output Leakage Current	V _{OUT} = 0V to OV _{DD}	● -10		10	μA
I _{SOURCE}	Output Source Current	V _{OUT} = 0V		-10		mA
I _{SINK}	Output Sink Current	V _{OUT} = OV _{DD}		10		mA

POWER REQUIREMENTS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD}	Supply Voltage		● 2.375	2.5	2.625	V
OV _{DD}	Supply Voltage		● 1.71		5.25	V
I _{VDD}	Supply Current	250ksps Sample Rate	●	2.1	2.5	mA
I _{OVDD}	Supply Current	250ksps Sample Rate (C _L = 20pF)	●	0.1		mA
I _{PD}	Power Down Mode	Conversion Done (I _{VDD} + I _{OVDD} + I _{REF})	●	1	90	μA
P _D	Power Dissipation	250ksps Sample Rate		5.25	6.25	mW
	Power Down Mode	Conversion Done (I _{VDD} + I _{OVDD} + I _{REF})		2.5	225	μW

ADC TIMING CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f _{SAMPL}	Maximum Sampling Frequency		●		250	ksps
t _{CONV}	Conversion Time		● 2		3	μs
t _{ACQ}	Acquisition Time	t _{ACQ} = t _{CYC} - t _{HOLD} (Note 10)	● 3.312			μs
t _{HOLD}	Maximum Time Between Acquisitions		●		688	ns
t _{CYC}	Time Between Conversions		● 4			μs
t _{CNVH}	CNV High Time		● 20			ns
t _{BUSYLH}	CNV to BUSY Delay	C _L = 20pF	●		13	ns
t _{CNVL}	Minimum Low Time for CNV	(Note 11)	● 20			ns
t _{QUIET}	SCK Quiet Time from CNV	(Note 10)	● 20			ns
t _{SCK}	SCK Period	(Notes 11, 12)	● 10			ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{SCKH}	SCK High Time		●	4		ns
t_{SCKL}	SCK Low Time		●	4		ns
t_{SSDISCK}	SDI Setup Time From SCK	(Note 11)	●	4		ns
t_{HSDISCK}	SDI Hold Time From SCK	(Note 11)	●	1		ns
t_{SCKCH}	SCK Period in Chain Mode	$t_{\text{SCKCH}} = t_{\text{SSDISCK}} + t_{\text{DSDO}}$ (Note 11)	●	13.5		ns
t_{DSDO}	SDO Data Valid Delay from SCK	$C_L = 20\text{pF}$, $OV_{\text{DD}} = 5.25\text{V}$ $C_L = 20\text{pF}$, $OV_{\text{DD}} = 2.5\text{V}$ $C_L = 20\text{pF}$, $OV_{\text{DD}} = 1.71\text{V}$	●		7.5	ns
			●		8	ns
			●		9.5	ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK	$C_L = 20\text{pF}$ (Note 10)	●	1		ns
$t_{\text{DSDOBUSYL}}$	SDO Data Valid Delay from BUSY	$C_L = 20\text{pF}$ (Note 10)	●		5	ns
t_{EN}	Bus Enable Time After RDL	(Note 11)	●		16	ns
t_{DIS}	Bus Relinquish Time After RDL	(Note 11)	●		13	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may effect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or OV_{DD} , they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latch-up.

Note 4: $V_{\text{DD}} = 2.5\text{V}$, $OV_{\text{DD}} = 2.5\text{V}$, $\text{REF} = 5\text{V}$, $V_{\text{CM}} = 2.5\text{V}$, $f_{\text{SMPL}} = 250\text{kHz}$, $\text{REF}/\text{DGC} = V_{\text{REF}}$.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero-scale error is the offset voltage measured from -0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of $-FS$ or $+FS$ untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale $\pm 5\text{V}$ input with a 5V reference voltage.

Note 9: $f_{\text{SMPL}} = 250\text{kHz}$, I_{REF} varies proportionately with sample rate.

Note 10: Guaranteed by design, not subject to test.

Note 11: Parameter tested and guaranteed at $OV_{\text{DD}} = 1.71\text{V}$, $OV_{\text{DD}} = 2.5\text{V}$ and $OV_{\text{DD}} = 5.25\text{V}$.

Note 12: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising capture.

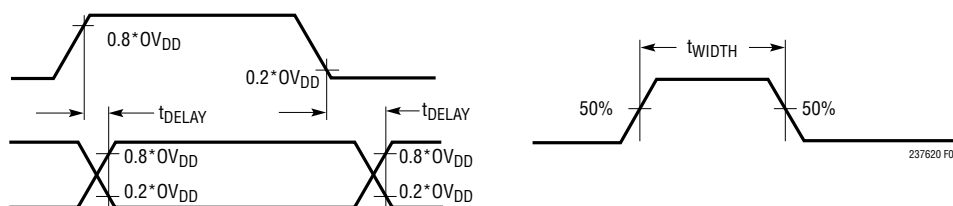
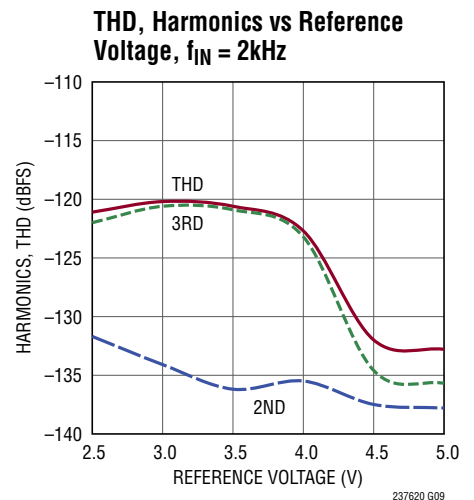
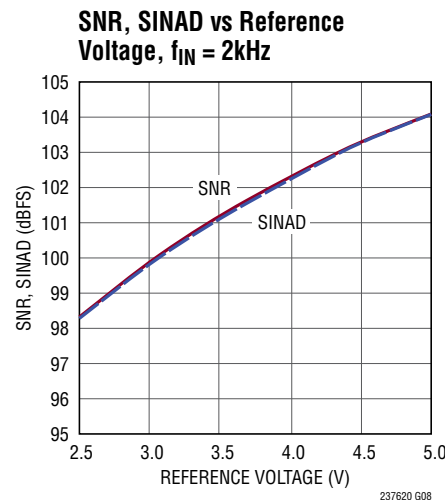
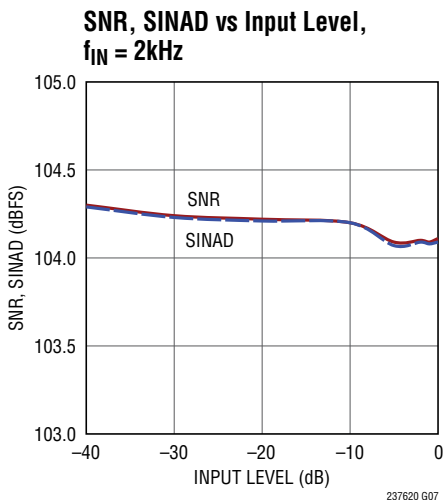
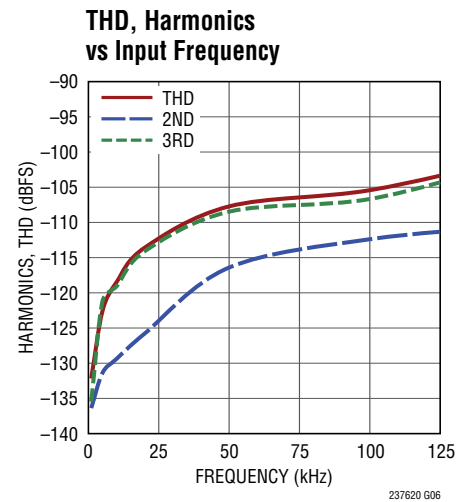
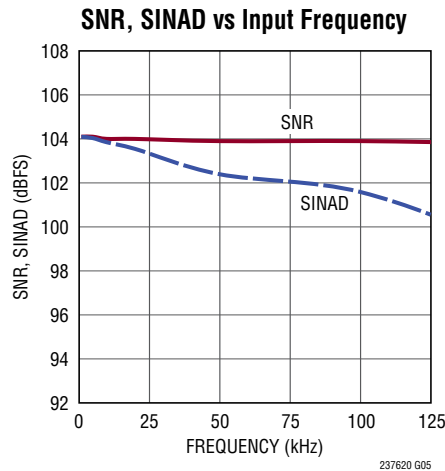
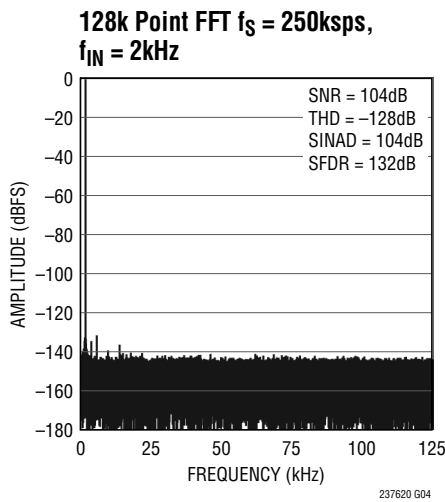
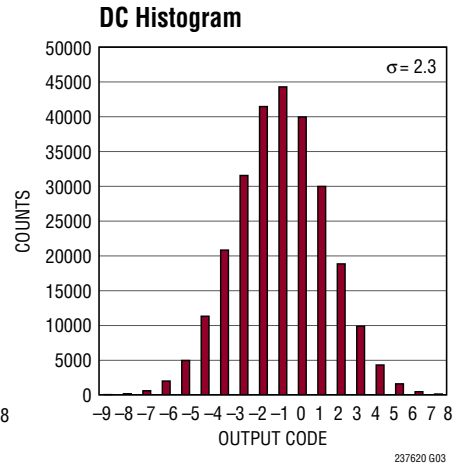
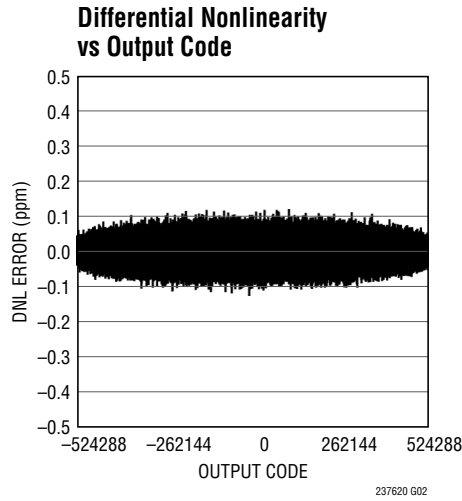
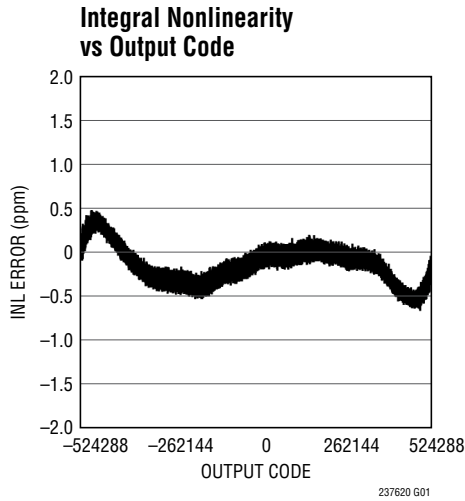


Figure 1. Voltage Levels for Timing Specifications

LTC2376-20

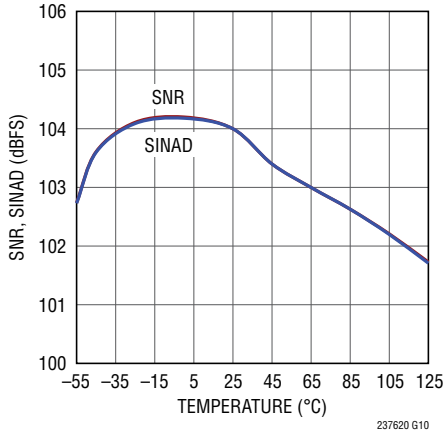
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{DD} = 2.5\text{V}$, $0V_{DD} = 2.5\text{V}$, $V_{CM} = 2.5\text{V}$, REF = 5V, $f_{SAMPL} = 250\text{kpsps}$, unless otherwise noted.



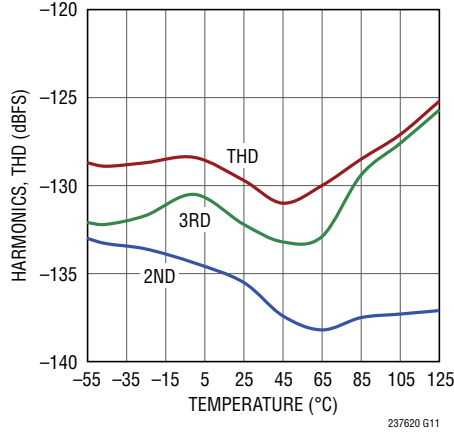
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TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{DD} = 2.5\text{V}$, $I_{OVD} = 2.5\text{V}$, $V_{CM} = 2.5\text{V}$,
 $REF = 5\text{V}$, $f_{SAMPL} = 250\text{ksps}$, unless otherwise noted.

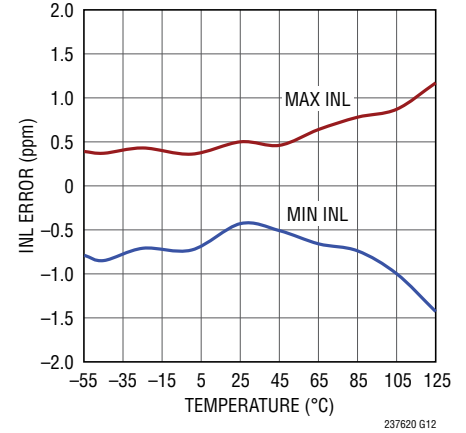
SNR, SINAD vs Temperature,
 $f_{IN} = 2\text{kHz}$



THD, Harmonics vs Temperature,
 $f_{IN} = 2\text{kHz}$



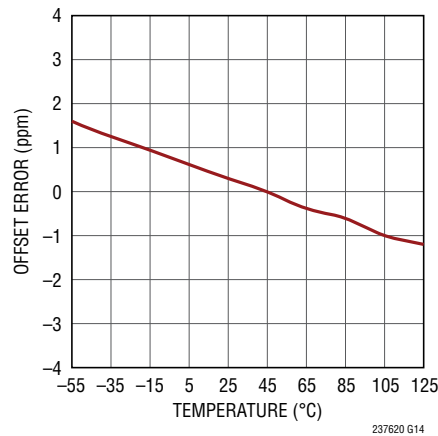
INL vs Temperature



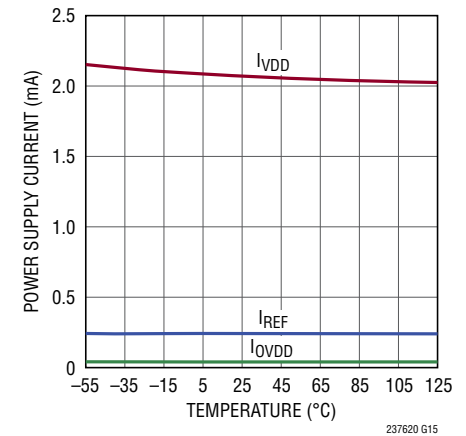
Full-Scale Error vs Temperature



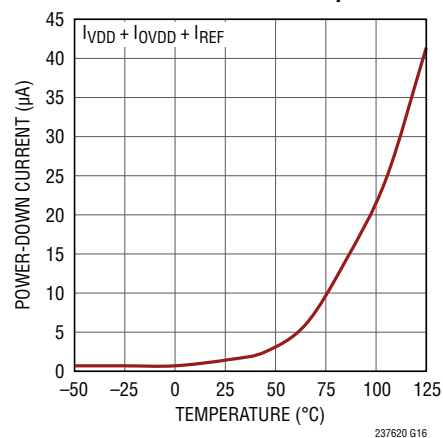
Offset Error vs Temperature



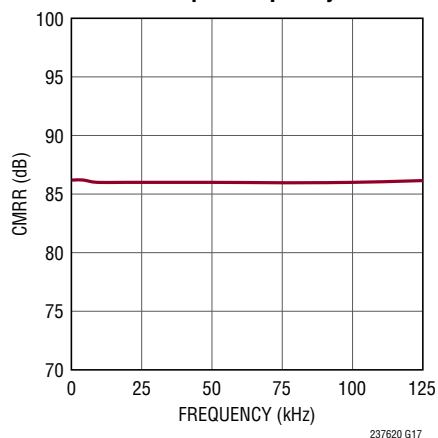
Supply Current vs Temperature



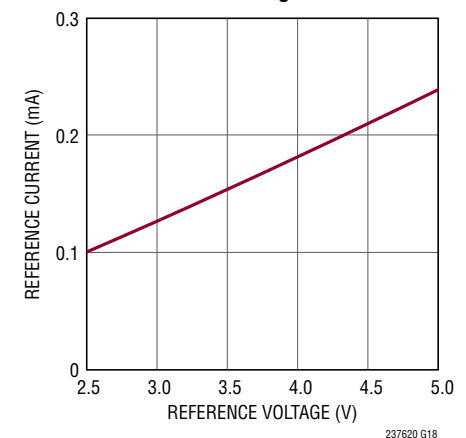
Shutdown Current vs Temperature



CMRR vs Input Frequency



Reference Current vs Reference Voltage



PIN FUNCTIONS

CHAIN (Pin 1): Chain Mode Selector Pin. When low, the LTC2376-20 operates in normal mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2376-20 operates in chain mode and the RDL/SDI pin functions as SDI, the daisy-chain serial data input. Logic levels are determined by OV_{DD} .

V_{DD} (Pin 2): 2.5V Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10 μ F ceramic capacitor.

GND (Pins 3, 6, 10 and 16): Ground.

IN^+ , IN^- (Pins 4, 5): Positive and Negative Differential Analog Inputs.

REF (Pin 7): Reference Input. The range of REF is 2.5V to 5.1V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47 μ F ceramic capacitor (X7R, 1210 size, 10V Rating).

REF/ \overline{DGC} (Pin 8): When tied to REF, digital gain compression is disabled and the LTC2376-20 defines full-scale according to the $\pm V_{REF}$ analog input range. When tied to GND, digital gain compression is enabled and the LTC2376-20 defines full-scale with inputs that swing between 10% and 90% of the $\pm V_{REF}$ analog input range.

CNV (Pin 9): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD} .

BUSY (Pin 11): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD} .

RDL/SDI (Pin 12): When CHAIN is low, the part is in normal mode and the pin is treated as a bus enabling input. When CHAIN is high, the part is in chain mode and the pin is treated as a serial data input pin where data from another ADC in the daisy chain is input. Logic levels are determined by OV_{DD} .

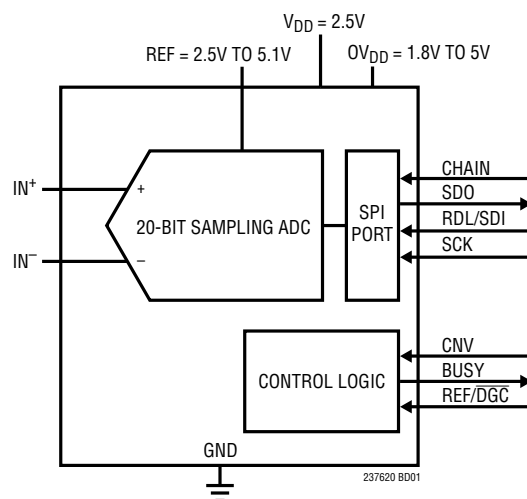
SCK (Pin 13): Serial Data Clock Input. When SDO is enabled, the conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSB first. Logic levels are determined by OV_{DD} .

SDO (Pin 14): Serial Data Output. The conversion result or daisy-chain data is output on this pin on each rising edge of SCK MSB first. The output data is in 2's complement format. Logic levels are determined by OV_{DD} .

OV_{DD} (Pin 15): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1 μ F capacitor.

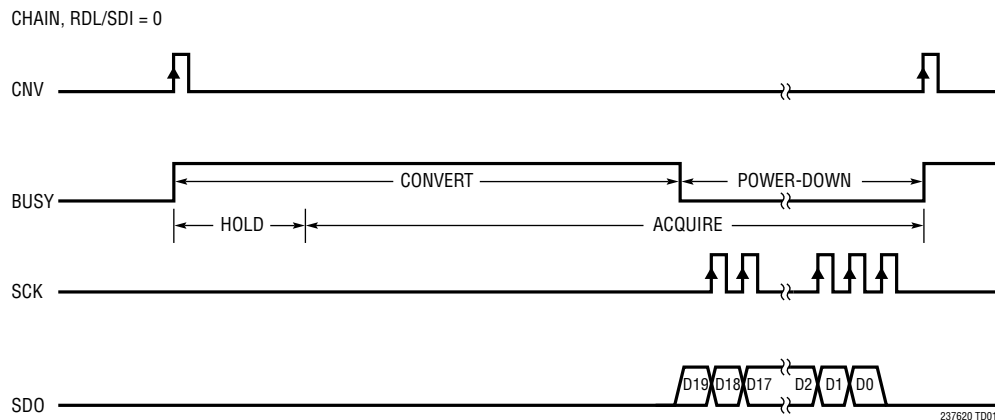
GND (Exposed Pad Pin 17 – DFN Package Only): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Conversion Timing Using the Serial Interface



APPLICATIONS INFORMATION

OVERVIEW

The LTC2376-20 is a low noise, low power, high speed 20-bit successive approximation register (SAR) ADC. Operating from a single 2.5V supply, the LTC2376-20 supports a large and flexible $\pm V_{REF}$ fully differential input range with V_{REF} ranging from 2.5V to 5.1V, making it ideal for high performance applications which require a wide dynamic range. The LTC2376-20 achieves ± 2 ppm INL maximum, no missing codes at 20 bits and 104dB SNR.

Fast 250ksps throughput with no cycle latency makes the LTC2376-20 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2376-20 dissipates only 5.3mW at 250ksps, while an auto power-down feature is provided to further reduce power dissipation during inactive periods.

The LTC2376-20 features a unique digital gain compression (DGC) function, which eliminates the driver amplifier's negative supply while preserving the full resolution of the ADC. When enabled, the ADC performs a digital scaling function that maps zero-scale code from $0V$ to $0.1 \cdot V_{REF}$ and full-scale code from V_{REF} to $0.9 \cdot V_{REF}$. For a typical reference voltage of 5V, the full-scale input range is now 0.5V to 4.5V, which provides adequate headroom for powering the driving amplifier from a single 5.5V supply.

CONVERTER OPERATION

The LTC2376-20 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the differential analog input voltage. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 20-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4$... $V_{REF}/1048576$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 20-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2376-20 digitizes the full-scale voltage of $2 \times REF$ into 2^{20} levels, resulting in an LSB size of $9.5\mu V$ with $REF = 5V$. Note that 1 LSB at 20 bits is approximately 1ppm. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

ANALOG INPUT

The analog inputs of the LTC2376-20 are fully differential in order to maximize the signal swing that can be digitized. The analog inputs can be modeled by the equivalent circuit

APPLICATIONS INFORMATION

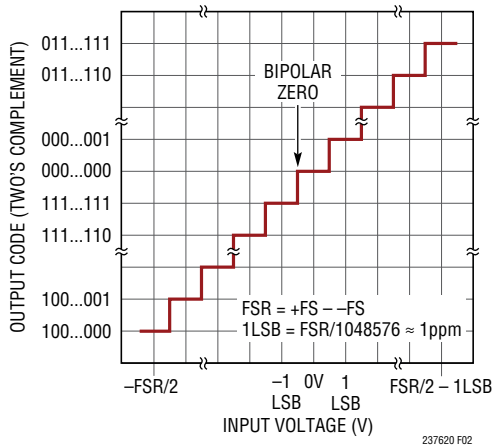


Figure 2. LTC2376-20 Transfer Function

shown in Figure 3. The diodes at the input provide ESD protection. In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC. The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2376-20 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2376-20. The amplifier provides low output impedance, which produces fast settling of the analog

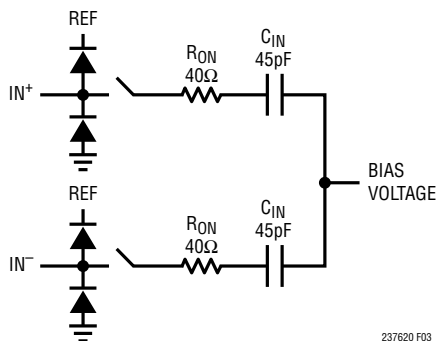


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2376-20

signal during the acquisition phase. It also provides isolation between the signal source and the ADC input currents.

Noise and Distortion

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.

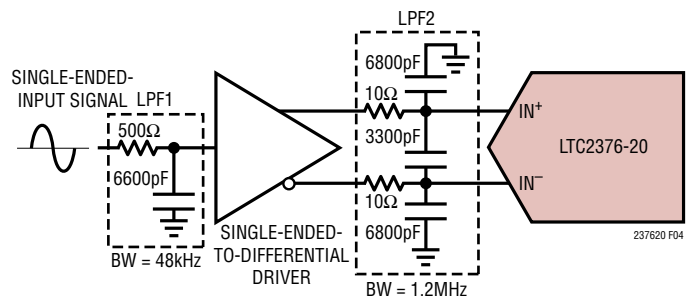


Figure 4. Input Signal Chain

A coupling filter network (LPF2) should be used between the buffer and ADC input to minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer. A buffer amplifier with a low noise density must be selected to minimize degradation of the SNR.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2376-20 is in dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase.

APPLICATIONS INFORMATION

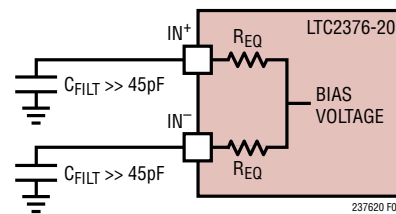
The ADC inputs may be modeled as a switched capacitor load of the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors (C_{FILT}) placed directly at the ADC inputs, and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled – This case is characterized by filter time constants and an overall settling time that is considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2376-20), the disturbance will not contribute any error.

Partially Settled – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high-frequency energy before it reaches the amplifier.

Fully Averaged – If the coupling filter capacitors (C_{FILT}) at the ADC inputs are much larger than the ADC's sample capacitors (45pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 250ksps, the equivalent input resistance is approximately 89k (as shown in Figure 5), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and the ADC's equivalent (switched-capacitor) input resistance, thus producing a gain error.

The input leakage currents of the LTC2376-20 should also be considered when designing the input drive circuit, because source impedances will convert input leakage currents to an added input voltage error. The input leakage currents, both common mode and differential, are typically extremely small over the entire operating temperature range. Figure 6 shows input leakage currents over temperature for a typical part.



$$R_{\text{EQ}} = \frac{1}{f_{\text{SMPL}} \cdot 45\text{pF}}$$

Figure 5. Equivalent Circuit for the Differential Analog Input of the LTC2376-20 at 250ksps.

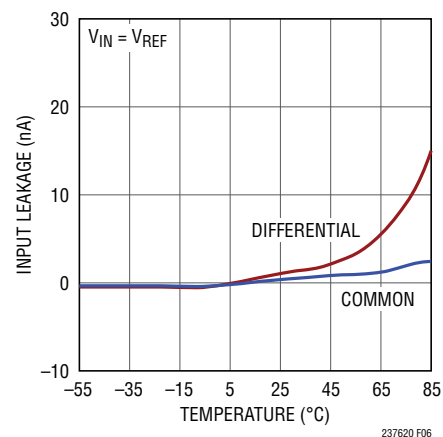


Figure 6. Common Mode and Differential Input Leakage Current Over Temperature

Let R_{S1} and R_{S2} be the source impedances of the differential input drive circuit shown in Figure 7, and let I_{L1} and I_{L2} be the leakage currents flowing out of the ADC's analog inputs. The voltage error, V_E , due to the leakage currents can be expressed as:

$$V_E = \frac{R_{S1} + R_{S2}}{2} \cdot (I_{L1} - I_{L2}) + (R_{S1} - R_{S2}) \cdot \frac{I_{L1} + I_{L2}}{2}$$

APPLICATIONS INFORMATION

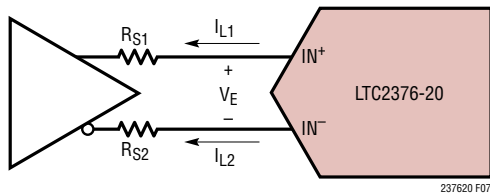


Figure 7. Source Impedances of a Driver and Input Leakage Currents of the LTC2376-20

The common mode input leakage current, $(I_{L1} + I_{L2})/2$, is typically extremely small (Figure 6) over the entire operating temperature range and common mode input voltage range. Thus, any reasonable mismatch (below 5%) of the source impedances R_{S1} and R_{S2} will cause only a negligible error. The differential input leakage current, $(I_{L1} - I_{L2})$, depends on temperature and is maximum when $V_{IN} = V_{REF}$, as shown in Figure 6. The differential leakage current is also typically very small, and its nonlinear component is even smaller. Only the nonlinear component will impact the ADC's linearity.

For optimal performance, it is recommended that the source impedances, R_{S1} and R_{S2} , be between 10Ω and 50Ω and with 1% tolerance. For source impedances in this range, the voltage and temperature coefficients of R_{S1} and R_{S2} are usually not critical. The guaranteed AC and DC specifications are tested with 10Ω source impedances, and the specifications will gradually degrade with increased source impedances due to incomplete settling of the inputs.

Fully Differential Inputs

A low distortion fully differential signal source driven through the LT6203 configured as two unity gain buffers

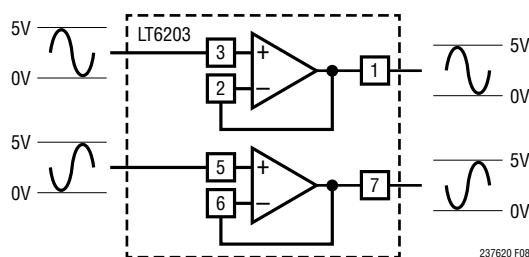


Figure 8. LT6203 Buffering a Fully Differential Signal Source

as shown in Figure 8 can be used to get the full data sheet distortion performance of -125dB .

Single-Ended-to-Differential Conversion

For single-ended input signals, a single-ended-to-differential conversion circuit must be used to produce a differential signal at the inputs of the LTC2376-20. The LT6203 ADC driver is recommended for performing single-ended-to-differential conversions. The LT6203 is flexible and may be configured to convert single-ended signals of various amplitudes to the $\pm 5\text{V}$ differential input range of the LTC2376-20.

Figure 9a shows the LT6203 being used to convert a 0V to 5V single-ended input signal. In this case, the first amplifier is configured as a unity gain buffer and the single-ended

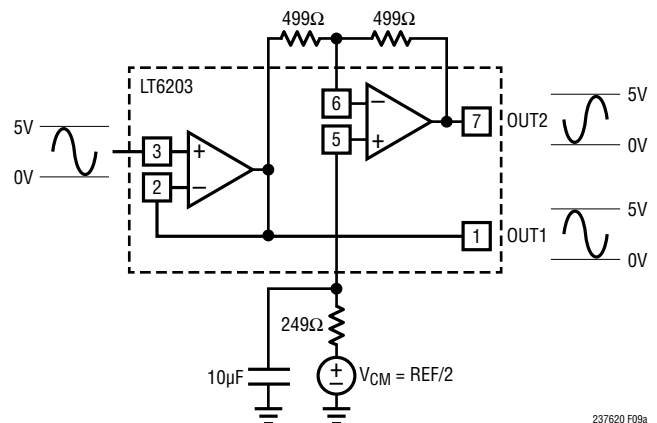


Figure 9a. LT6203 Converting a 0V to 5V Single-Ended Signal to a $\pm 5\text{V}$ Differential Input Signal

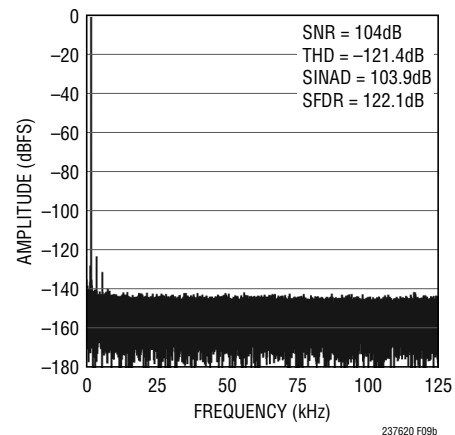


Figure 9b. 128k Point FFT Plot with $f_{IN} = 2\text{kHz}$ for Circuit Shown in Figure 9a

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1. However, less gain is sufficient if the amplifier's gain characteristic is known to be (mostly) linear. An amplifier's offset versus signal level must be considered for amplifiers configured as unity gain buffers. For example, 1ppm linearity may require that the offset is known to vary less than 5 μ V for a 5V swing. However, greater offset variations may be acceptable if the relationship is known to be (mostly) linear. Unity-gain buffer amplifiers typically require substantial headroom to the power supply rails for best performance. Inverting amplifier circuits configured to minimize swing at the amplifier input terminals may perform better with only little headroom than unity-gain buffer amplifiers. The linearity and thermal properties of an inverting amplifier's feedback network should be considered carefully to ensure DC accuracy.

ADC REFERENCE

The LTC2376-20 requires an external reference to define its input range. A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2376-20. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/ $^{\circ}$ C (max) temperature coefficient for high precision applications.

When choosing a bypass capacitor for the LTC6655-5, the capacitor's voltage rating, temperature rating, and package size should be carefully considered. Physically larger capacitors with higher voltage and temperature ratings tend to provide a larger effective capacitance, better filtering the noise of the LTC6655-5, and consequently producing a higher SNR. Therefore, we recommend bypassing the LTC6655-5 with a 47 μ F ceramic capacitor (X7R, 1210 size, 10V rating) close to the REF pin.

The REF pin of the LTC2376-20 draws charge (Q_{CONV}) from the 47 μ F bypass capacitor during each conversion cycle. The reference replenishes this charge with a DC current, $I_{REF} = Q_{CONV}/t_{CYC}$. The DC current draw of the REF pin, I_{REF} , depends on the sampling rate and output code. If the LTC2376-20 is used to continuously sample a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5LSBs.

When idling, the REF pin on the LTC2376-20 draws only a small leakage current (< 1 μ A). In applications where a burst of samples is taken after idling for long periods as shown in Figure 12, I_{REF} quickly goes from approximately 0 μ A to a maximum of 0.3mA at 250ksps. This step in DC current draw triggers a transient response in the reference that must be considered since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-5 reference is also recommended.

DYNAMIC PERFORMANCE

Fast Fourier Transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2376-20 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling

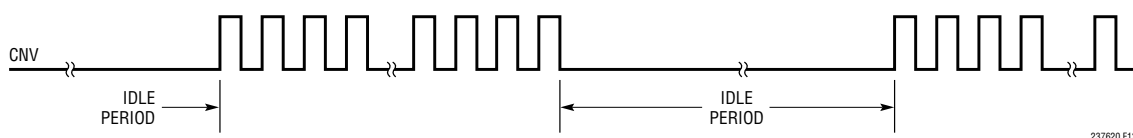


Figure 12. CNV Waveform Showing Burst Sampling

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frequency. Figure 13 shows that the LTC2376-20 achieves a typical SINAD of 104dB at a 250kHz sampling rate with a 2kHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and

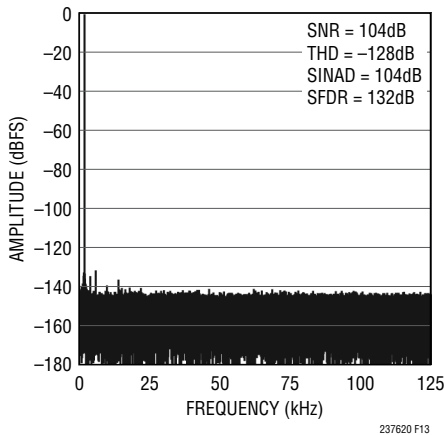


Figure 13. 128k Point FFT Plot with $f_{IN} = 2\text{kHz}$ of the LTC2376-20

the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 13 shows that the LTC2376-20 achieves a typical SNR of 104dB at a 250kHz sampling rate with a 2kHz input.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SAMPL}/2$). THD is expressed as:

$$\text{THD} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2376-20 provides two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2376-20 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2376-20 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2376-20 has a power-on-reset (POR) circuit that will reset the LTC2376-20 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 200 μs after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

CNV Timing

The LTC2376-20 conversion is controlled by CNV. A rising edge on CNV will start a conversion and power up the LTC2376-20. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed.

Acquisition

A proprietary sampling architecture allows the LTC2376-20 to begin acquiring the input signal for the next conversion 675ns after the start of the current conversion. This

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extends the acquisition time to $3.312\mu\text{s}$, easing settling requirements and allowing the use of extremely low power ADC drivers. (Refer to the Timing Diagram.)

Internal Conversion Clock

The LTC2376-20 has an internal clock that is trimmed to achieve a maximum conversion time of $3\mu\text{s}$.

Auto Power-Down

The LTC2376-20 automatically powers down after a conversion has been completed and powers up once a new conversion is initiated on the rising edge of CNV. During power down, data from the last conversion can be clocked out. To minimize power dissipation during

power down, disable SDO and turn off SCK. The auto power-down feature will reduce the power dissipation of the LTC2376-20 as the sampling frequency is reduced. Since power is consumed only during a conversion, the LTC2376-20 remains powered-down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 14.

DIGITAL INTERFACE

The LTC2376-20 has a serial digital interface. The flexible OV_{DD} supply allows the LTC2376-20 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

The serial output data is clocked out on the SDO pin when an external clock is applied to the SCK pin if SDO is enabled. Clocking out the data after the conversion will yield the best performance. With a shift clock frequency of at least 20MHz, a 250kps throughput is still achieved. The serial output data changes state on the rising edge of SCK and can be captured on the falling edge or next rising edge of SCK. D19 remains valid until the first rising edge of SCK.

The serial interface on the LTC2376-20 is simple and straightforward to use. The following sections describe the operation of the LTC2376-20. Several modes are provided depending on whether a single or multiple ADCs share the SPI bus or are daisy chained.

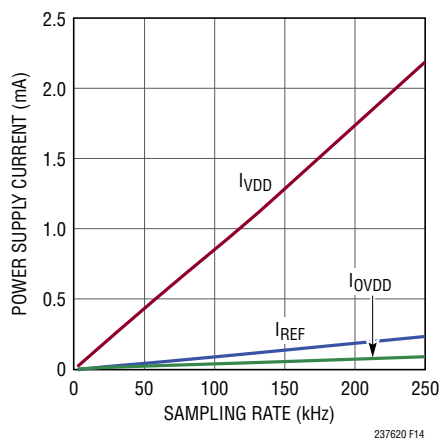


Figure 14. Power Supply Current of the LTC2376-20 Versus Sampling Rate

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Normal Mode, Single Device

When CHAIN = 0, the LTC2376-20 operates in normal mode. In normal mode, RDL/SDI enables or disables the serial data output pin SDO. If RDL/SDI is high, SDO is in high impedance. If RDL/SDI is low, SDO is driven.

Figure 15 shows a single LTC2376-20 operated in normal mode with CHAIN and RDL/SDI tied to ground. With RDL/SDI grounded, SDO is enabled and the MSB(D19) of the new conversion data is available at the falling edge of BUSY. This is the simplest way to operate the LTC2376-20.

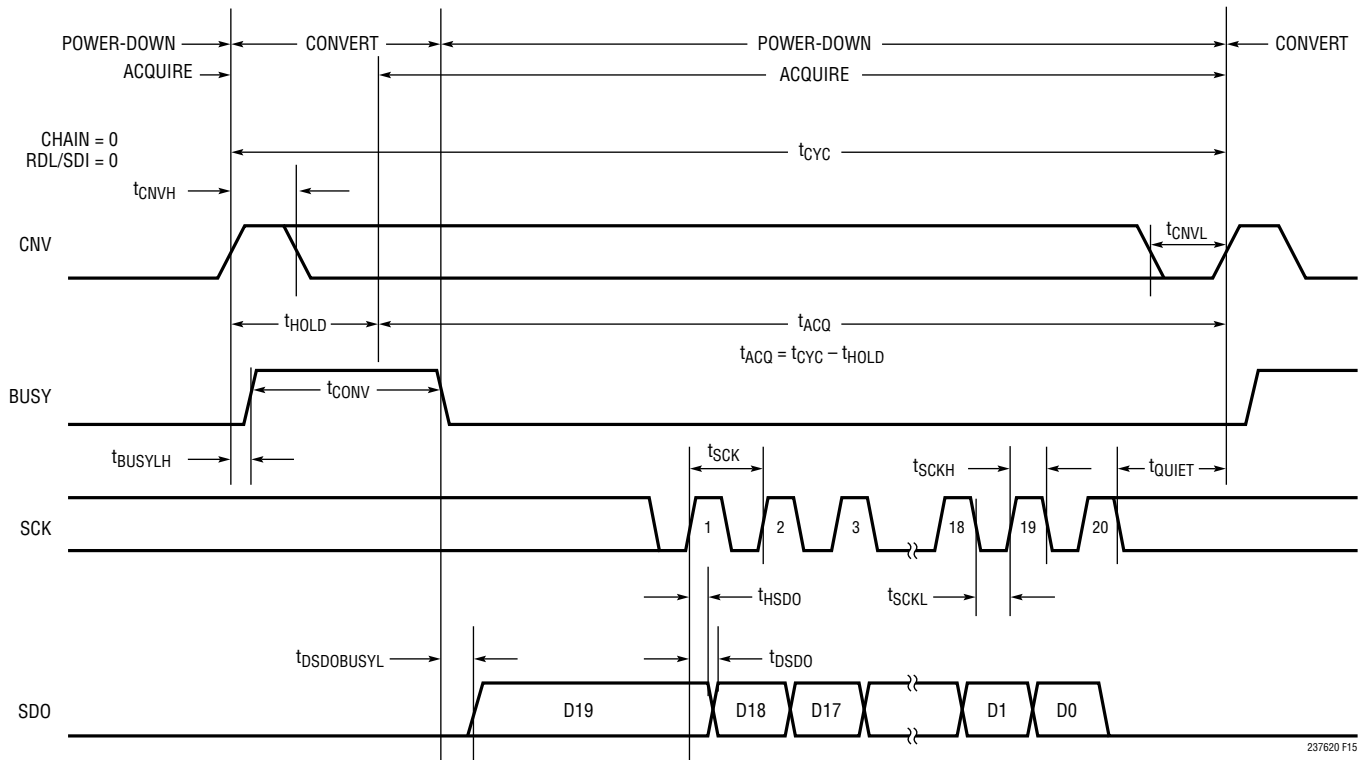
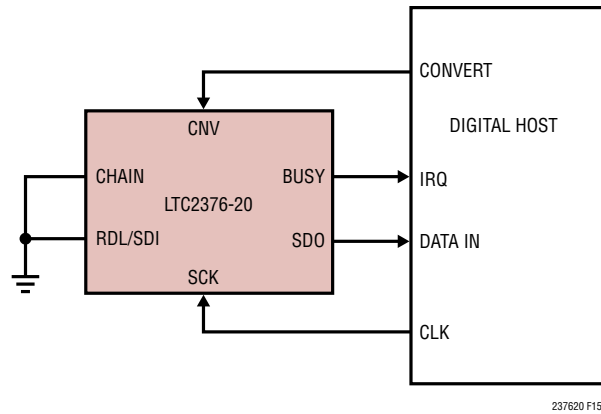


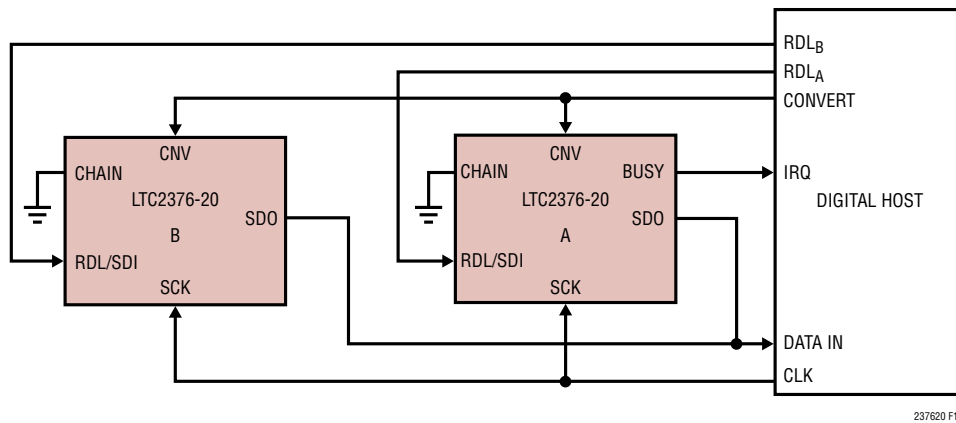
Figure 15. Using a Single LTC2376-20 in Normal Mode

APPLICATIONS INFORMATION

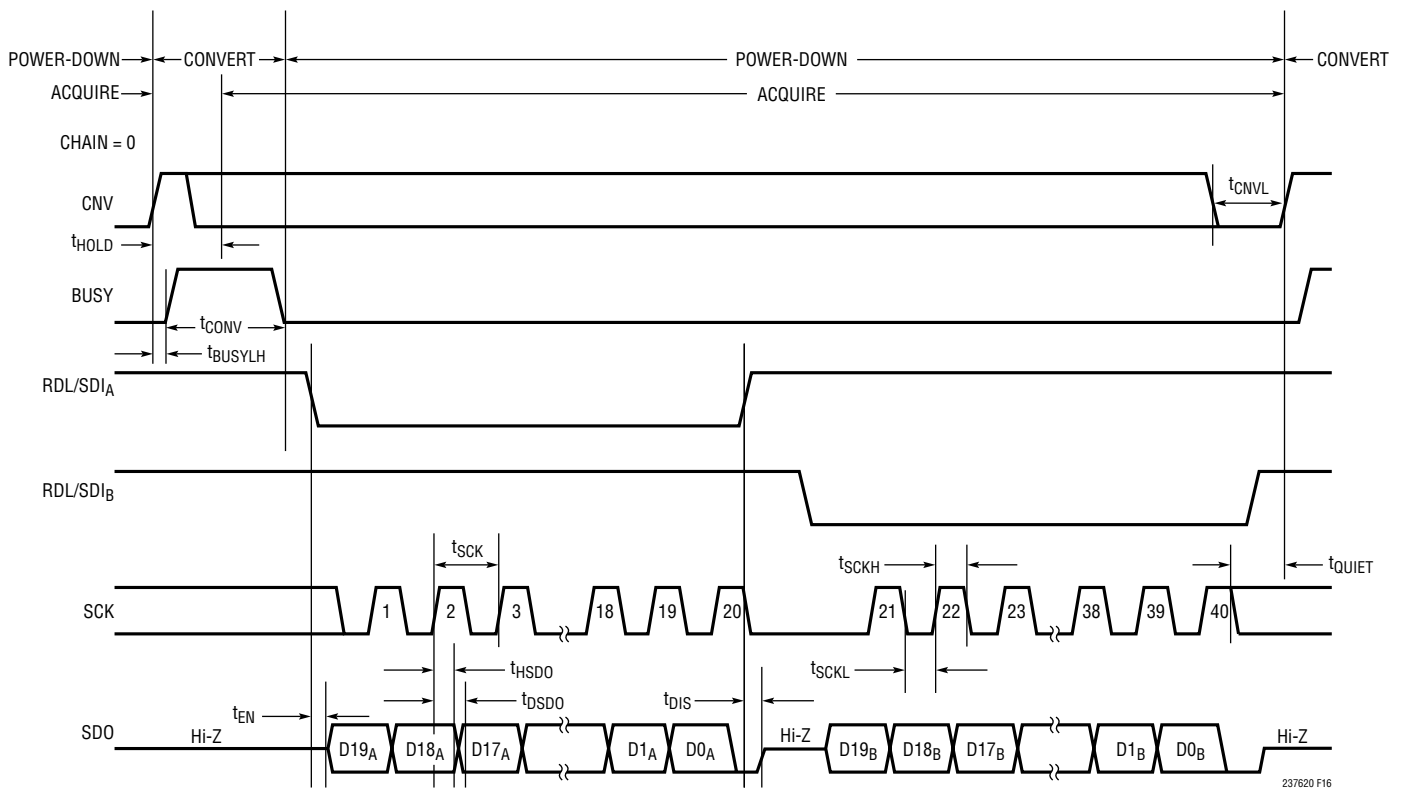
Normal Mode, Multiple Devices

Figure 16 shows multiple LTC2376-20 devices operating in normal mode (CHAIN = 0) sharing CNV, SCK and SDO. By sharing CNV, SCK and SDO, the number of required signals to operate multiple ADCs in parallel is reduced.

Since SDO is shared, the RDL/SDI input of each ADC must be used to allow only one LTC2376-20 to drive SDO at a time in order to avoid bus conflicts. As shown in Figure 16, the RDL/SDI inputs idle high and are individually brought low to read data out of each device between conversions. When RDL/SDI is brought low, the MSB of the selected device is output onto SDO.



237620 F16a



237620 F16

Figure 16. Normal Mode With Multiple Devices Sharing CNV, SCK and SDO

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Chain Mode, Multiple Devices

When $CHAIN = OV_{DD}$, the LTC2376-20 operates in chain mode. In chain mode, SDO is always enabled and RDL/SDI serves as the serial data input pin (SDI) where daisy-chain data output from another ADC can be input.

This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. Figure 17 shows an example with two daisy-chained devices. The MSB of converter A will appear at SDO of converter B after 20 SCK cycles. The MSB of converter A is clocked in at the SDI/RDL pin of converter B on the rising edge of the first SCK.

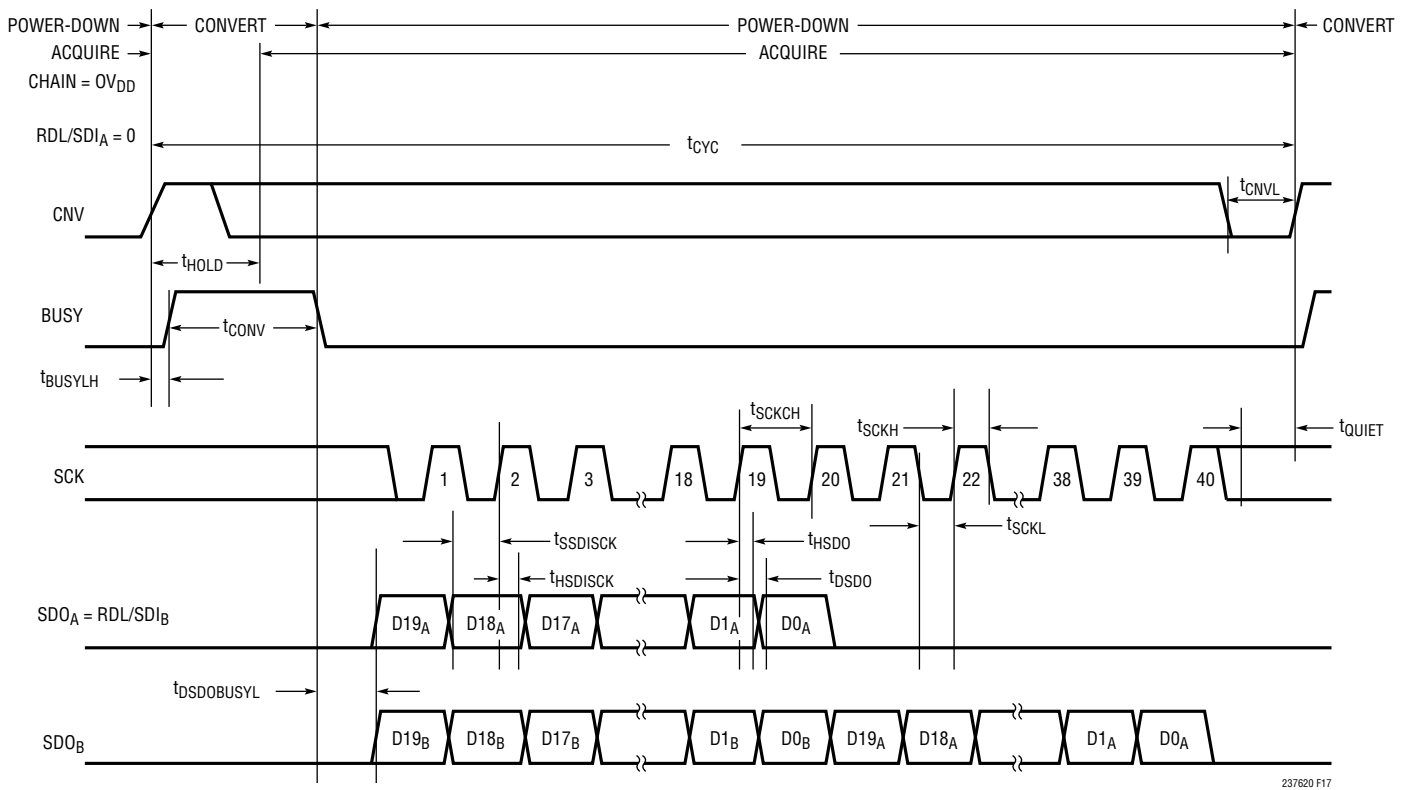
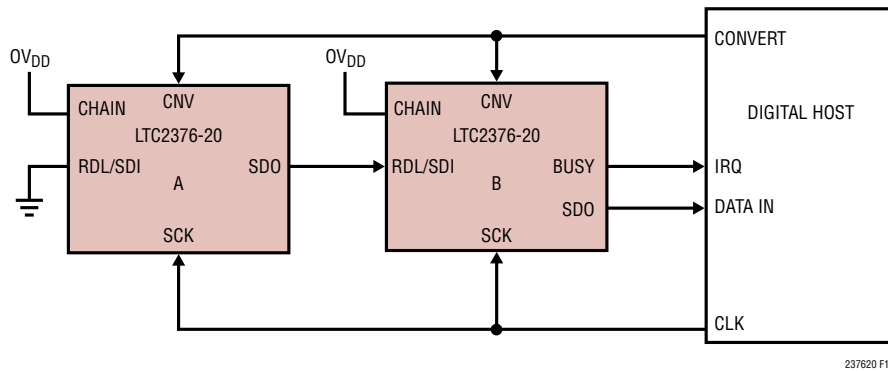


Figure 17. Chain Mode Timing Diagram

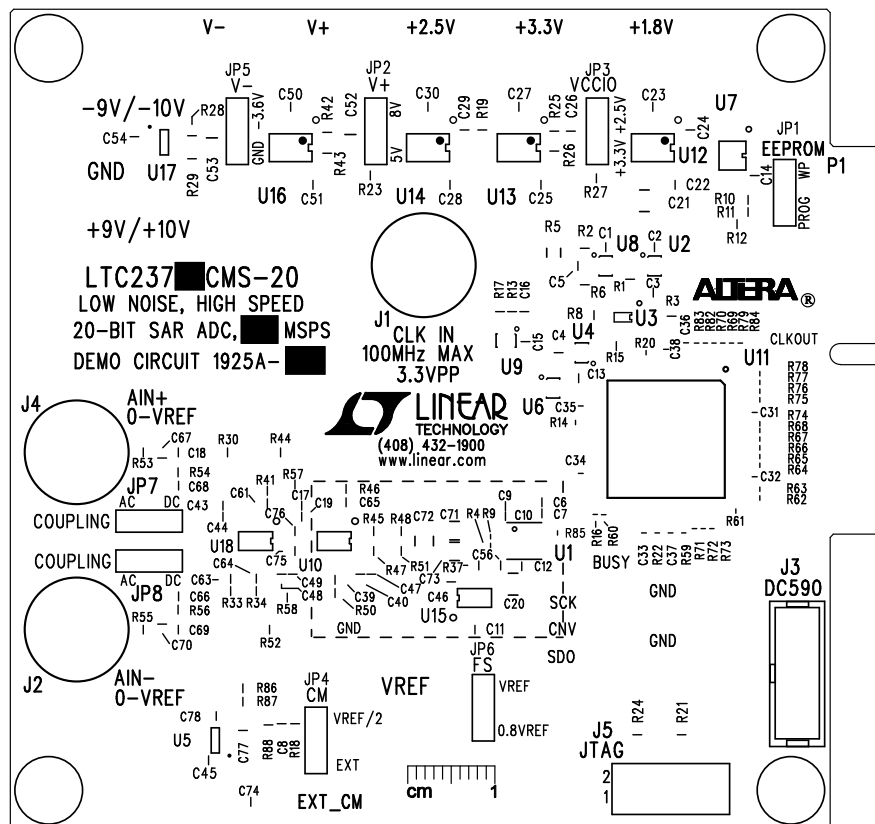
BOARD LAYOUT

To obtain the best performance from the LTC2376-20 a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Recommended Layout

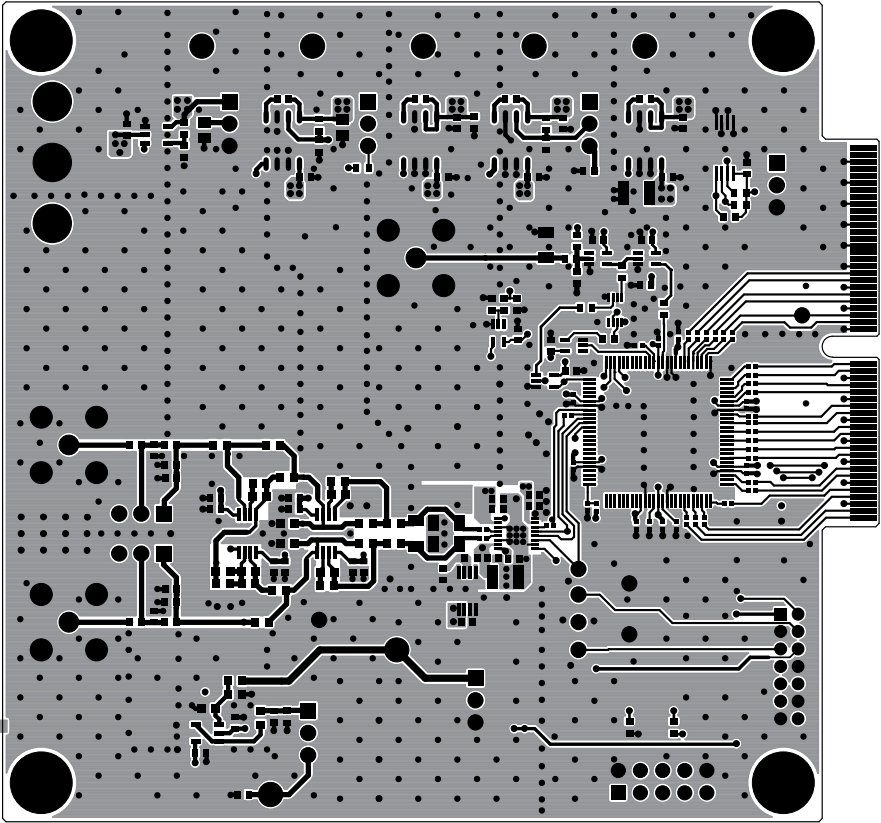
The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1925A, the evaluation kit for the LTC2376-20.

Top Silkscreen



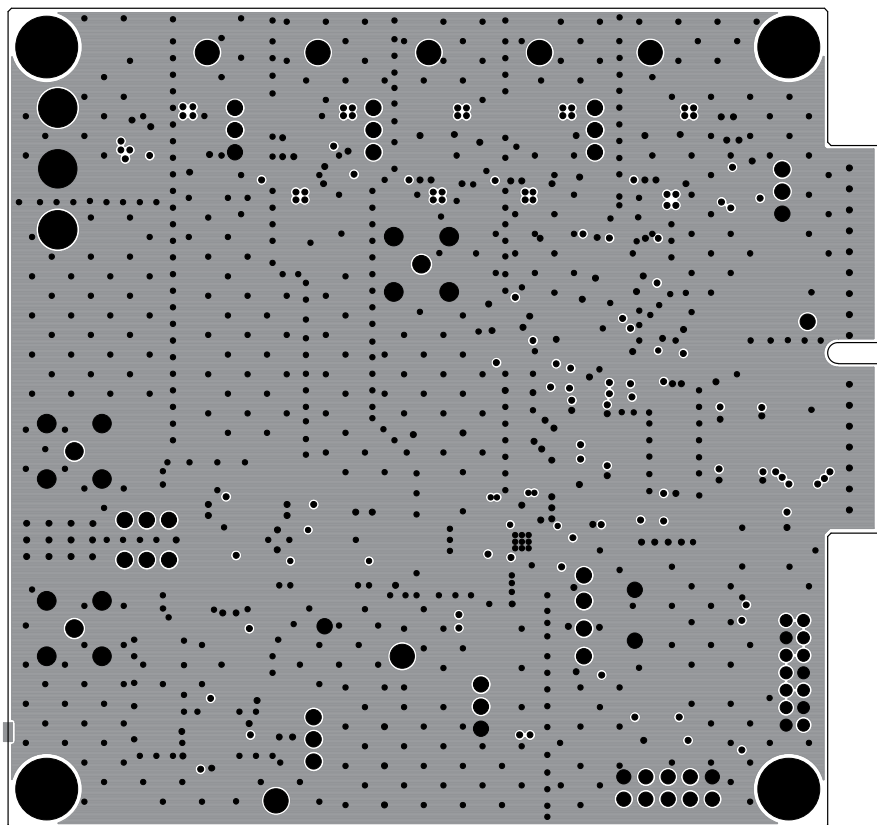
BOARD LAYOUT

Layer 1 Component Side



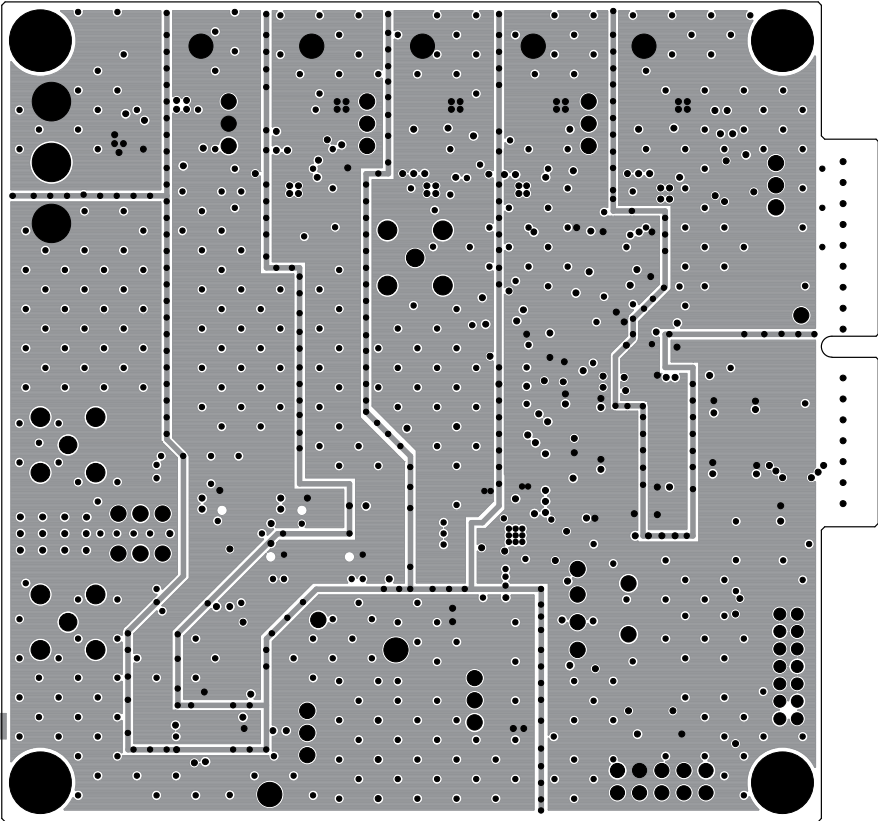
BOARD LAYOUT

Layer 2 Ground Plane



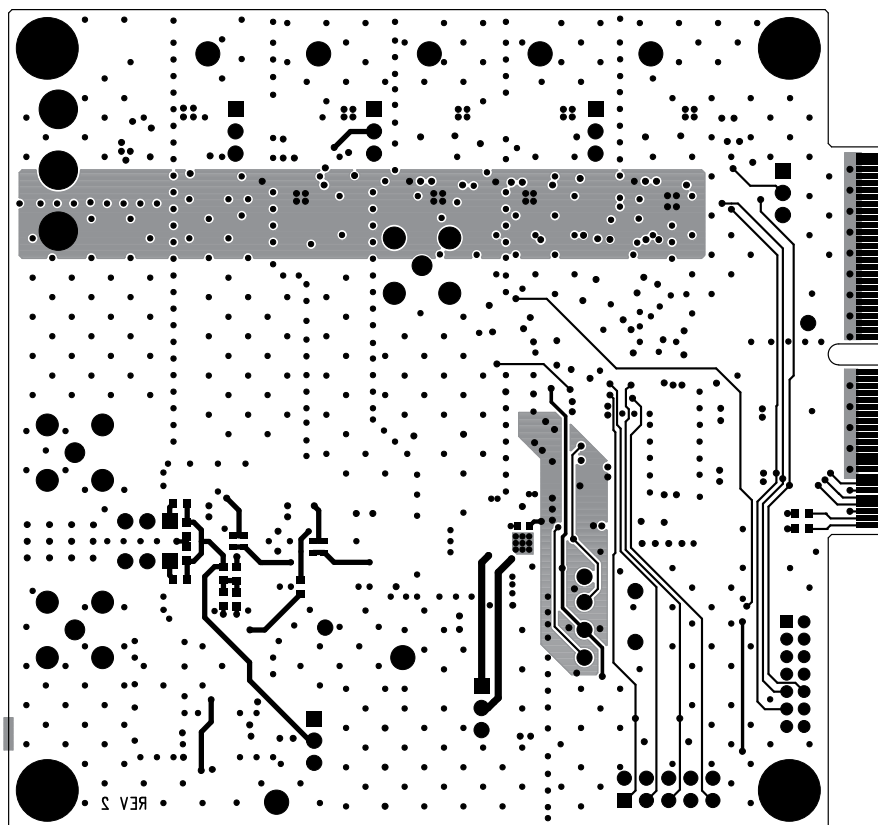
BOARD LAYOUT

Layer 3 PWR Plane



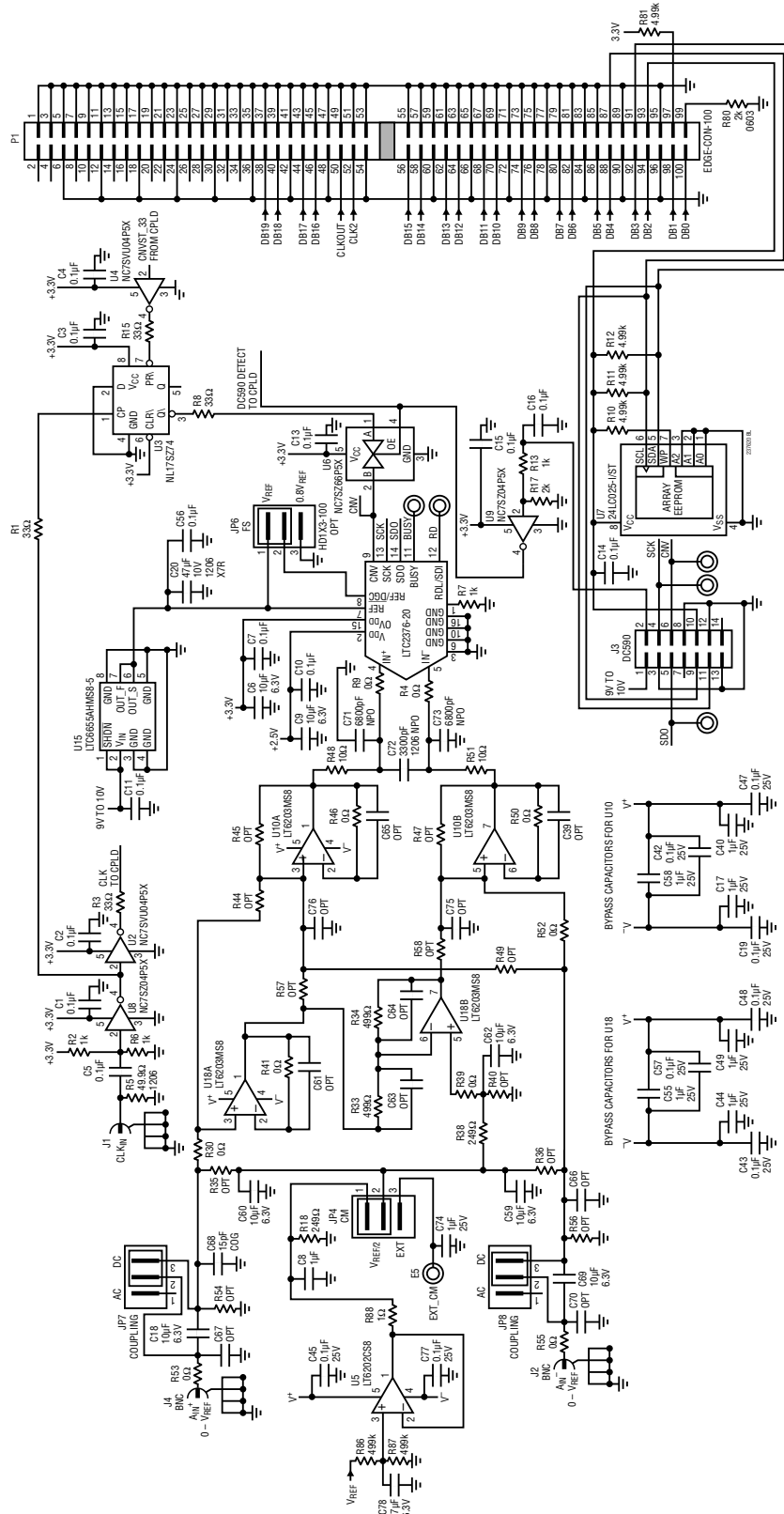
BOARD LAYOUT

Layer 4 Bottom Layer



BOARD LAYOUT

Partial Schematic of Demoboard

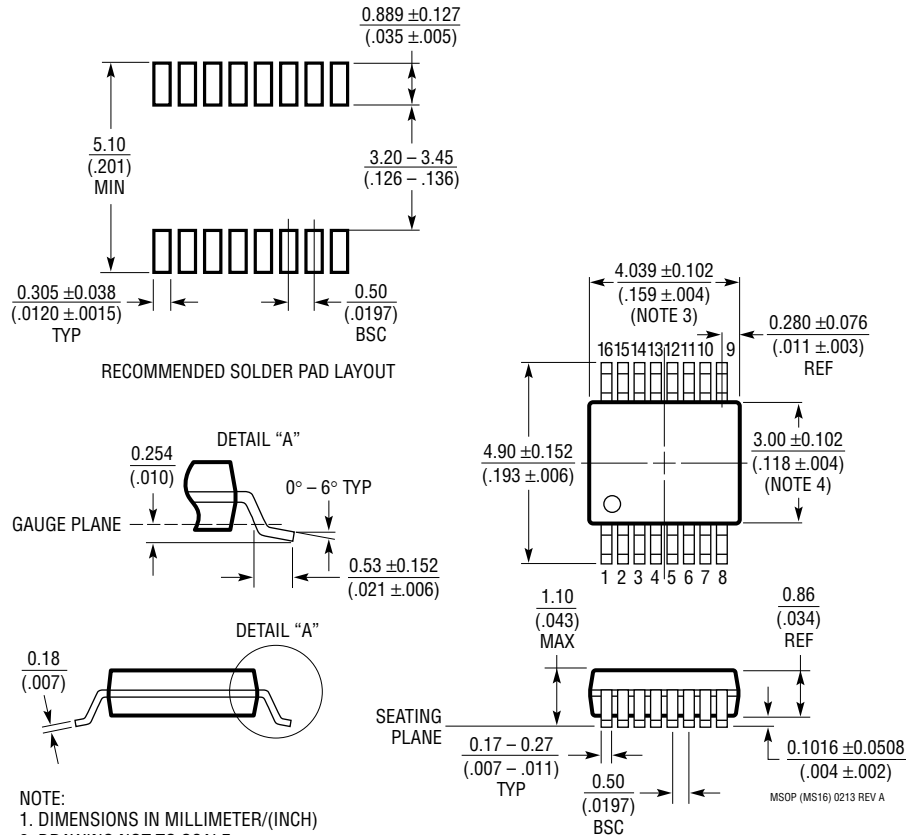


PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2376-20#packaging> for the most recent package drawings.

MS Package 16-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1669 Rev A)



- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
 2. DRAWING NOT TO SCALE
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
 5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/15	Corrected a typo in the schematic of Figure 11a and Typical Application	14 and 30
B	08/16	Updated graphs TA02, G01, G02, and G03	1 and 6

